Program the SAME Here and Over There – Intel® Data Parallel Programming Models and Intel® Many Integrated Core Architecture

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SFTS005
Agenda

• **Overview**
  - Intel® Many Integrated Core Architecture (Intel® MIC Architecture) and Complementing Software Stack
  - Models of Computation
  - Intel® Xeon® Processor + Intel MIC Architecture: Writing Code for Today and Tomorrow

• **Intel® Parallel Composer**
  - Seamless Data Parallel: Turning “Small Knobs” to Run on Intel MIC Architecture
  - Array Notations
  - Carry Over Vectorization to Many Cores

• **Intel® Array Building Blocks**
  - C++ Library Front-End to Specify Arbitrary Data-Parallel Computation
  - Virtual Machine API to Create New Front-Ends

• **Programming for Intel MIC Architecture Without Using Offload**

• **Summary and Q&A**

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URL is on top of Session Agenda Pages in Pocket Guide
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Overview – A Step Forward in Performance with Excellent Programmability

First product to coincide with 22nm process codenamed Knights Corner

**Delivered Performance**

Launching on 22nm with >50 cores to provide outstanding performance for HPC users

**Performance Density**

The compute density associated with specialty accelerators for parallel workloads

**Programmability**

The many benefits of broad Intel® processor programming models, techniques, and familiar x86 developer tools
Develop Using Parallel Models that Support Heterogeneous Computing

C/C++
- Intel® Parallel Building Blocks
- Intel® Cilk™ Plus
  - Intel® Threading Building Blocks
  - Intel® Array Building Blocks
- Offload pragmas
- OpenMP*
- OpenCL*

Fortran
- Co-array
- Offload directives
- OpenMP

The complementing software stack is common to both multicore and Many-core
Invest in Common Tools and Programming Models

**Multicore**

Intel® Xeon® processors are designed for intelligent performance and smart energy efficiency.

Continuing to advance Intel Xeon processor family and instruction set (e.g., Intel® Advanced Vector Extensions, etc.)

**Your Application**

**Many-core**

Intel® MIC Architecture - Co-processor ideal for highly parallel computing applications

Software development platforms ramping now

We extend Intel’s Development Tools for Intel® Many Integrated Core Products
Versatile Models of Computation for Intel® Many Integrated Core Products

Intel® MIC Architecture integrates full-featured processor cores and can either act as a coprocessor or host for applications.
Program for Multicore Today...
Be Ready for Intel® Many Integrated Core Products

Source

Compilers Libraries, Parallel Models

Multicore CPU

Multicore CPU

Intel MIC architecture co-processor

Multicore Cluster

Clusters with Multicore and Many-core

Multicore

Many-core

Clusters

Eliminate Need for Dual Programming Architecture
**Intel® Xeon® Processors + Intel® MIC Products: What happens with and without the coprocessor?**

<table>
<thead>
<tr>
<th>Without: Intel® MIC Architecture Co-processor(s) are absent</th>
<th>With: Intel MIC Architecture Co-processor(s) are present</th>
</tr>
</thead>
<tbody>
<tr>
<td>Application starts and executes on host</td>
<td>Application starts on host and executes portions on Intel MIC Co-processor(s)</td>
</tr>
<tr>
<td>At runtime, if Intel® MIC Co-processor(s) are available, the target binary is loaded</td>
<td>At each offload, the construct runs on the Intel MIC Co-processor(s)</td>
</tr>
<tr>
<td>At each offload, the construct runs on host cores/threads</td>
<td></td>
</tr>
<tr>
<td>Normal program termination on host</td>
<td>At program termination, target binary is unloaded</td>
</tr>
</tbody>
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*Intel® Many Integrated Core Architecture = Intel® MIC Architecture*
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Replicate data-parallel task with cilk_for, cilk_spawn Keywords

Vectorize with Intel® Cilk™ Plus data parallelism

Offload with _Offload_cilk_for, _Offload_cilk_spawn

Intel® Many Integrated Core Architecture (Intel® MIC Architecture)
From Intel® Xeon® to Intel® MIC Products: Seamless Data Parallelism

- Write architecture portable vector code with Intel® Cilk™ Plus Extensions
- No knowledge of Intel® Streaming SIMD Extensions, Advanced Vector Extensions or Intel® Many Integrated Core Instructions needed
- Same code can be recompiled to target different architectures
Intel® Cilk™ Plus Array Notation: Simple and Powerful Vectorization

- Use a “::” in array subscripts to operate on multiple elements
  - A[:]
    // all of array A
  - A[lower_bound : length]
  - A[lower_bound : length : stride]

Examples
- float A[64]; // Declare C/C++ array A as 64 floats
- A[:]
  // All elements of array A
  // Elements 2 to 7 of A
- A[0:3:2]
  // Elements 0,2,4 of A
Operations on Array Sections

- **C/C++ operators**

  ```
c[:,:,] = a[3:2][3:2] + b[5:2][5:2]; // 2x2 array addition
  // sizes and "ranks" in assignments must be the same
  ```

- **Function calls**

  ```
b[:] = foo(a[:]); // Call foo() on each element of a[]
  // Need builtin, inlining or elemental function for
  // vectorization
  ```

- **Reductions combine array elements to get a single result**

  ```
  sum = __sec_reduce_add(a[:]); // Add all elements of a
  // many other reductions: all_zero, all_non_zero, max, min, // etc.
  ```

- **If-then-else and conditional operators allow masked operations**

  ```
  if (mask[:]) {
      a[:] = b[:];
  }
  ```
Elemental Functions

- A different style of writing vector code
- The compiler automatically vectorizes an entire function
- Single data elements are turned into vectors

```c
__declspec(vector) float cxpy(float a, float x, float y) {
    return a*x + y;  // a, x, y are turned into vectors
}
```

```c
float a[64],x[64],y[64],r[64];
r[:]=cxpy(a[:],x[:],y[:]);  // Can use a for-loop instead
```

- On Intel® AVX, the above code will generate a `cxpy()` that processes 8 elements of the arrays at a time
- The caller will send data to `cxpy()` in groups of 8
- Can specify scalar parameters, linear-increasing, etc.
Data Parallelism with Intel® Cilk™ Plus is Easier!

```c
void foo(float* dest, short* src, long len, float a) {
    dest[0:len] = ((float) src[0:len]) * a;
}

or

__declspec(vector,scalar(a))
float foo(float dest, short src, long len, float a) {
    dest = src * a;
}
```

VS.

```c
#include <pmmintrin.h>

void foo(float* dest, short* src, long len, float a) {
    __m128 xmmMul = _mm_set1_ps(a);

    for(long i = 0; i < len; i+=4) {
        __m128i xmmSrc1i = _mm_loadl_epi64((__m128i*) &src[i]);
        xmmSrc1i = _mm_cvtepi16_epi32(xmmSrc1i);
        __m128 xmmSrc1f = _mm_cvtepi32_ps(xmmSrc1i);
        xmmSrc1f = _mm_mul_ps(xmmSrc1f, xmmMul);
        _mm_store_ps(&dest[i], xmmSrc1f);
    }
```

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Task Parallelism with Intel® Cilk™ Plus

// Example 1
cilk_for (int y = 0; y < height; y++) {
    render_one_line(y);
}

// Example 2
buffer = cilk_spawn load_image("1.jpg");
buffer2 = load_image("2.jpg");

• Create parallel for-loops or function calls
• Runtime maps tasks to system threads
Offloading to Intel® MIC Products: Simple, easy, and works with your C/C++ code

- Use `_Offload_cilk_for`, `_Offload_cilk_spawn`

- Your data-parallel code is optimized for Intel® MIC products and offloaded to the engine

- Compiler handles data transfer between host and “offload space”
  - We also offer keywords for optional user control

- Use our language features to write parallel code, and the tools put it where it needs to go!
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Intel® Array Building Blocks (Intel® ArBB)
Ideal for data parallel programming

- A generalized vector parallel programming solution
- Ideal for applications requiring data-intensive mathematical computations

```cpp
//Simple per element multiplication using Intel® ArBB:

void dotprod(const arbb::dense<arbb::f32>& a,
             const arbb::dense<arbb::f32>& b,
             arbb::dense<arbb::f32>& c)
{
    c = a * b;
}
```

Intel ArBB is applicable to multicore and many-core programming

Learn more at http://intel.com/go/arbb
How Does It Work?

**Sequentially consistent semantics**

<table>
<thead>
<tr>
<th>Component</th>
<th>Functionality</th>
</tr>
</thead>
</table>
| Intel® ArBB kernels in “serial” C++ app | - Templates
- Overloaded operators                                                  |
| Standard C++ compiler            | - Links with dynamic library                                                |
| Intel® ArBB Runtime              | - Dynamic compiler
- Threading and heterogeneous runtime                                         |

**Diagram:**

- **CPU**
- **Future**

Intel® Array Building Blocks (Intel® ArBB)
Containers

Regular Containers

- dense<T>
- dense<T, 3>
- array<...>
- struct user_type {
  ...
};
- Class user_type {
  ...
};

Irregular Containers

- dense<T, 2>
- nested<T>
- dense<array<...>>
- dense<user_type>
Vector Processing or Scalar Processing

dense<f32> A, B, C, D;
A = A + B/C * D;

void kernel(f32& a, f32 b, f32 c, f32 d) {
    a = a + (b/c)*d;
}
...
dense<f32> A, B, C, D;
map(kernel)(A, B, C, D);
Running on Intel® MIC Products?

• Intel® ArBB lib calls in app’s main() invoke JIT, which generates target code and invokes the runtime

• Target Host or Intel® MIC product with environment variable
  – MIC: ARBB_HETEROGENEOUS_MODEL=OFFLOAD_ONLY
  – CPU: ARBB_HETEROGENOUS_MODEL=HOST_ONLY

• JIT generates target code

• ARBB_NUM_CORES
  – Specifies the number of SW threads used as workers
  – Default setting is # cores
  – Can change from the API with arbb_set_num_threads

• Heterogeneous runtime (HRT)
  – Moves the MIC .so files for TBB and ArBB at initialization
  – Moves the code and input data per ArBB call
  – Invokes the remote code
  – Moves the output data back

• Remote runtimes
  – Threading (TRT)
  – Memory (MRT)
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Programming for Intel® Many Integrated Core Architecture without Offload
“Stand-alone” Intel MIC Computing

- Intel® MIC Architecture software environment includes a highly functional, general purpose OS running on the co-processor with:
  - A familiar Unix* flavored interactive shell
  - A file system that supports subdirectories, file reads, writes, etc.
  - standard i/o including printf
  - Virtual memory management
  - Process, thread management & scheduling
  - Interrupt and exception handling
  - Semaphores, mutexes, etc...

- What does this mean?
  - A large majority of existing code even with OS oriented calls like fork() can port with a simple recompile
  - Intel MIC Architecture natively supports parallel coding models like Intel® Cilk™ Plus, Intel® Threading Building Blocks, pThreads*, OpenMP*
Summary
What Makes a Great Model for Data Parallel?

Composable

• Portable
• Performance
• Safety
There are Many Parallel Programming Models for C, C++ and Fortran

*If you write good code, it can be applied to both Intel® Xeon® and Intel® Many Integrated Core Architecture*

<table>
<thead>
<tr>
<th>Intel® Parallel Building Blocks</th>
<th>Domain-Specific Libraries</th>
<th>Established Standards</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Intel® Cilk™ Plus</strong>&lt;br&gt;Language extensions to simply parallelism</td>
<td><strong>Intel® Integrated Performance Primitives</strong>&lt;br&gt;Widely used C++ template library for parallelism</td>
<td>Intel® Message Passing Interface (MPI) Library</td>
</tr>
<tr>
<td><strong>Intel® Threading Building Blocks</strong>&lt;br&gt;Widely used C++ Library for data parallelism</td>
<td><strong>Intel® Math Kernel Library</strong>&lt;br&gt;Powerful C++ Library for data parallelism</td>
<td>OpenMP*</td>
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<td><strong>Intel® Array Building Block</strong>&lt;br&gt;Powerful C++ Library for data parallelism</td>
<td></td>
<td>Fortran Coarray</td>
</tr>
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</table>

Mix and match to optimize your applications performance
Program for Multicore Today... Be Ready for Intel® Many Integrated Core Products

Source

Compilers Libraries, Parallel Models

Multicore CPU

Multicore CPU

Intel MIC architecture co-processor

Multicore Cluster

Clusters with Multicore and Many-core

Eliminate Need for Dual Programming Architecture
<table>
<thead>
<tr>
<th>Date</th>
<th>Event</th>
<th>Time</th>
<th>Location</th>
<th>Presenter(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Tuesday—September 13</strong></td>
<td>Demo—Intel® IDF Technology Showcase</td>
<td>5:00 p.m.–7:00 p.m.</td>
<td>Software Community area of the Technology Showcase</td>
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<td></td>
<td>Session - A Three-Pronged Approach to Improving Software Stability</td>
<td>11:20 a.m.–12:10 p.m.</td>
<td>Room 2011</td>
<td>David Mackay</td>
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<td>Using Intel® Software Correctness Tools</td>
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<td>Intel® Cluster Checker Tool – An Automated Approach and Extensible</td>
<td>1 p.m.–4:00 p.m.</td>
<td>Room 2000</td>
<td>Jeremy Siadal</td>
</tr>
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<td>Tool for Analyzing High-Performance Computing Clusters</td>
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<td>Task Parallel Evolution and Revolution—Intel® Cilk™ Plus and Intel®</td>
<td>2:10 p.m.–3:00 p.m.</td>
<td>Room 2011</td>
<td>Noah Clemons and Victoria Gromova</td>
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<td>Threading Building Blocks</td>
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<td></td>
<td>Program the SAME, Here and over There—Intel® Data Parallel Programming</td>
<td>3:20 p.m.–4:10 p.m.</td>
<td>Room 2011</td>
<td>Noah Clemons and Chang-Sun Lin, Jr.</td>
</tr>
</tbody>
</table>

| **Wednesday—September 14** | Demo—Intel® IDF Technology Showcase                                  | 11 a.m.–1 p.m. and 4 p.m.–7 p.m. | Software Community area of the Technology Showcase                      |                                        |
|                            | Embedded System Tools for Development and Validation of Intel® Atom™  | 11:20 a.m.–12:10 p.m. | Room 2011                                                                | Robert Mueller                         |
|                            | Processor-Based Devices                                               |                       |                                                                          |                                        |
|                            | Intel® Cluster Checker Tool – An Automated Approach and Extensible     | 1 p.m.–4:00 p.m.      | Room 2000                                                                | Jeremy Siadal                          |
|                            | Tool for Analyzing High-Performance Computing Clusters                 |                       |                                                                          |                                        |
|                            | Intel® Faces of Parallelism Lab: Parallel Models for Multi/Many Core   | 1:05 p.m.–5:05 p.m.   | Room 2010                                                                | Noah Clemons                          |
|                            | Intel® Cluster Checker Tool – An Automated Approach and Extensible     | 11 a.m.–2 p.m.        | Room 2000                                                                |                                        |
|                            | Tool for Analyzing High-Performance Computing Clusters                 | 4 p.m.–7 p.m.         |                                                                          |                                        |
|                            | Performance Profiling Secrets: The new Intel® VTune™ Amplifier XE for  | 2:05 p.m.–2:55 p.m.   | Room 2011                                                                | Shannon Cepeda                         |
|                            | Beginning and Experienced Tuners                                      |                       |                                                                          |                                        |
|                            | Parallel Programming Methods from an Intel and Microsoft® Perspective  | 2:05 p.m.–2:55 p.m.   | Room 2009                                                                | James Reinders and Steve Teixeira      |
|                            | Intel® Cluster Checker Tool – An Automated Approach and Extensible     | 1 p.m.–4:00 p.m.      | Room 2000                                                                | Jeremy Siadal                          |
|                            | Tool for Analyzing High-Performance Computing Clusters                 |                       |                                                                          |                                        |
|                            | Intel® Faces of Parallelism Lab: Parallel Models for Multi/Many Core   | 1:05 p.m.–5:05 p.m.   | Room 2010                                                                | Noah Clemons                          |
| **Thursday—September 15** | Demo—Intel® IDF Technology Showcase                                  | 11 a.m.–2 p.m.        | Software Community area of the Technology Showcase                      |                                        |
|                           | Intel® Cluster Checker Tool – An Automated Approach and Extensible     | 1 p.m.–4:00 p.m.      | Room 2000                                                                | Jeremy Siadal                          |
|                           | Tool for Analyzing High-Performance Computing Clusters                 |                       |                                                                          |                                        |
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Rev. 5/9/11